AMENDMENTS TO THE CLAIMS

1-47. (Canceled)

48. (Previously presented) ~~A display according to claim 25~~ A display comprising:

a display portion, said display portion having a plurality of gate lines, a plurality of signal lines and a plurality of pixels,

a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines; and

a plurality of driver circuits, said plurality of driver circuits including at least one general driver circuit and one remainder driver circuit,

each said at least one general driver circuit having a general driver horizontal shift register circuit and a plurality of general driver circuit output terminals, a general driver circuit output terminal of said plurality of general driver circuit output terminals providing a signal potential to one of said plurality of signal lines,

said remainder driver circuit having a remainder driver horizontal shift register circuit and a plurality of remainder driver circuit output terminals, a remainder driver circuit output terminal of said plurality of remainder driver circuit output terminals providing another signal potential to another of said plurality of signal lines,

the quantity of said remainder driver circuit output terminals being defined as (S – (OP * (DC-1))), "S" being the quantity of said plurality of signal lines, "OP" being the quantity of said general driver circuit output terminals, and "DC" being the quantity of said plurality of driver circuits, and

said quantity of said general driver circuit output terminals being different than said quantity of said remainder driver circuit output terminals,

wherein said plurality of driver circuits are driver integrated circuits arranged in an outside of a transparent insulating substrate on which said display portion is formed.

49-54. (Canceled)

55. (Currently amended) ~~A display according to claim 49, further comprising:~~ A display comprising:

a display portion, said display portion having a plurality of gate lines, a plurality of signal lines and a plurality of pixels;

a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines;

a plurality of driver circuits, each of said plurality of driver circuits having a plurality of driver circuit output terminals;

a driver circuit output terminal of said a plurality of driver circuit output terminals providing a signal potential to a signal line of said plurality of signal lines;

the quantity of said driver circuit output terminals being the same quantity for said each of said plurality of driver circuits;

the quantity of said driver circuits being defined as N/n, wherein "N" is the quantity of said signal lines and "n" is said quantity of said driver circuit output terminals;

a memory circuit for temporarily storing data to be written into said plurality of driver circuits; and

a control circuit for controlling said plurality of driver circuits so as to simultaneously write different data from said memory circuit.

56-78. (Canceled)